VSRV1: Simple 32-bit Linux RISC-V Core

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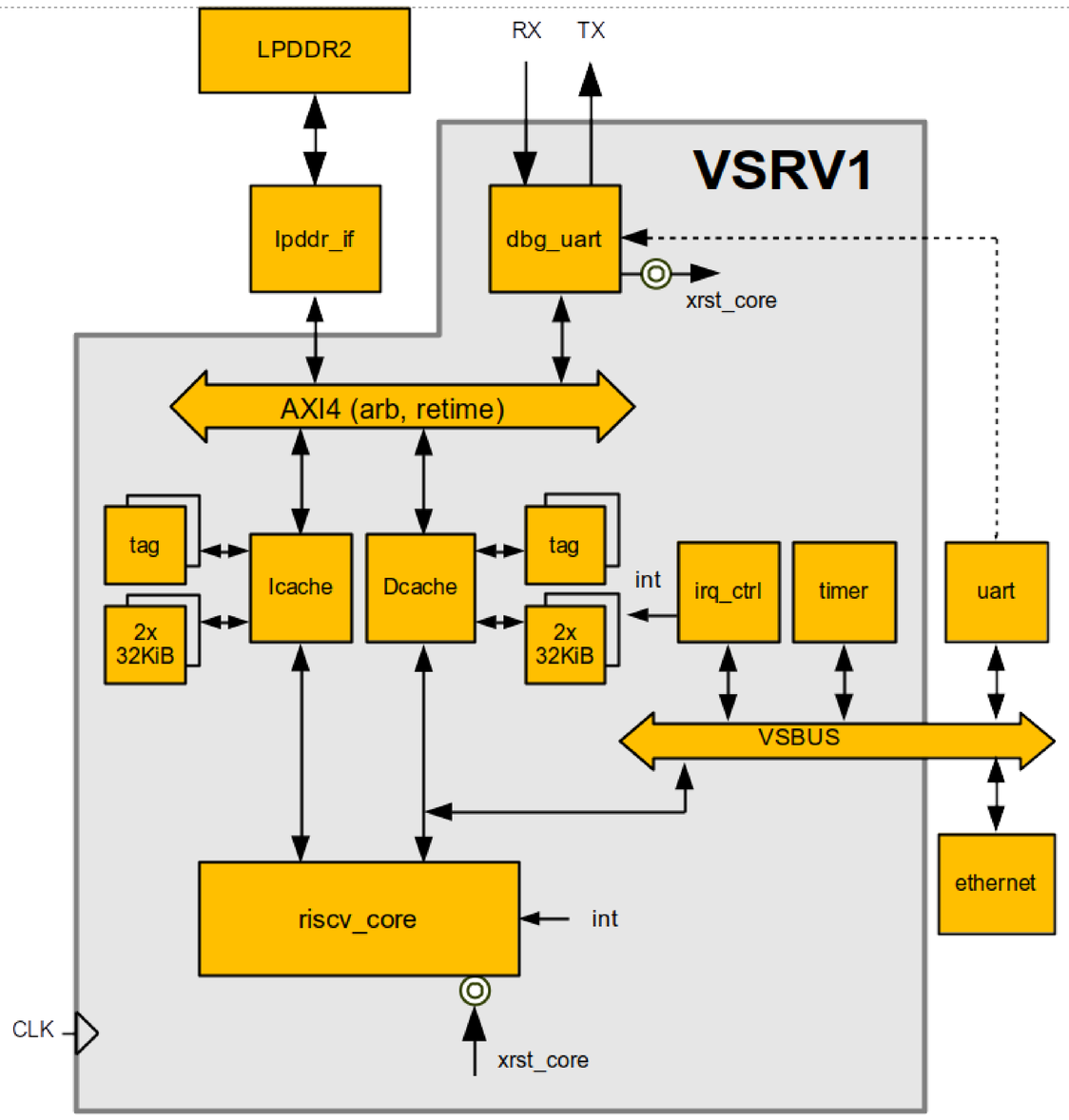
VLSI Solution Oy

Design Objectives of the VSRV1 Core

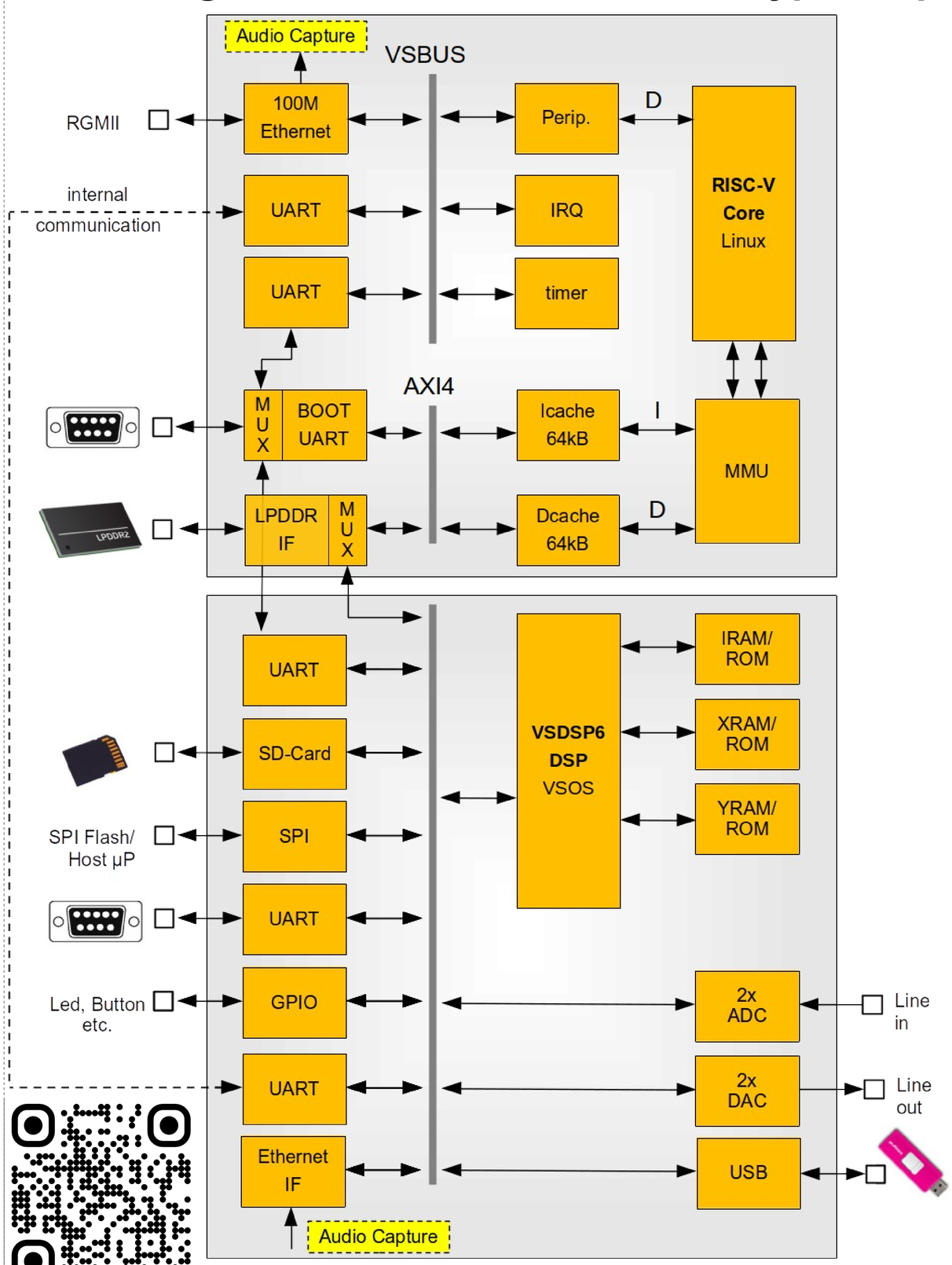
- Lightweight Linux capable RV32IM core
- Functions as interface protocol platform (e.g. ethernet protocol stack)
- Can be used for IoT
  → low power, Linux OS based applications
- Two-way set-associative cache
- Open source (to be released in github)



Performance Roadmap of the VSRV1 Core

Type	Clock MHz	Added Feature	Linux Boot Time / s	MIPS
FPGA	50	Starting point, 8KiB I-cache, no D-cache	250	3
FPGA	50	16KiB D-cache	78	12
FPGA	50	Half-Speed LPDDR2 Interface	43	18
FPGA	50	MMU TLB	25	24
FPGA	50	Full-Speed LPDDR2, 2x32KiB cache	17	35
Chip	100	VSRVES01 estimate 2x64KiB cache	8	77

Block Diagram of the VSRVES01 Prototype Chip



Silicon Area of the VSRV1 Core

Type	Size
cache	128KiB
registers	3471 instances
logic	22,278 equivalent Nand gates

Features of the VSRVES01 Prototype IC

- 100+MHz speed with 110nm MS technology
- High quality audio A/D and D/A
- Ethernet communication implemented with Linux software stack
- Ethernet HW can forward audio directly to the DSP processor
- Linux boot time from power-up less than 8s
- QFN-88 package (10x10x0.8mm)

Initial Target Applications:

- Real time audio over ethernet
- Ethernet controlled streaming audio player or recorder
- Speech synthesis

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